Patent No. 5,203,721. Applicant respectfully traverses these rejections for the following reasons.

Response to Rejections under 35 U.S.C. § 112, second paragraph

The Examiner contends that claims 1-23 fail to particularly point and distinctly claim the subject matter Applicant regards as the invention. More particularly, the Examiner alleges that the terms "the circumferential surface," "the outer circumferential surface," the outer circumferential direction," the longitudinal direction," and "the inner circumferential surface" lack antecedent basis. In response, Applicant amends claims 2-10, 12, and 14-23 to improve form by changing the term "the" to --a-- or --an-- where appropriate. In view of this, Applicant requests withdrawal of the 35 U.S.C. § 112, second paragraph, rejection.

Additionally, the Examiner alleges that the phrase "outer circumferential direction" recited in claim 14 is ambiguous. In response, Applicant amends claim 14 to clarify the subject matter recited therein. In view of this, Applicant requests withdrawal of the 35 U.S.C. § 112, second paragraph, rejection.

Response to Rejections under 35 U.S.C. § 102(b)

The Examiner contends that Sharp anticipates claims 1-11, 13, 16, 17, 20, 24, and 26 and that Buck anticipates claims 1, 12, 13, 14, 18, 19, and 21-23. In order to properly anticipate Applicant's claimed invention under 35 U.S.C. § 102(b), each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131 (8th Ed., Aug. 2001), quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Finally, "[t]he elements must be

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arranged as required by the claim." M.P.E.P. § 2131 p. 2100-69. Applicant respectfully submits that neither Sharp nor Buck alone teaches all the claim elements.

I. **Sharp**

Claim 1 of the present invention is directed to a semiconductor device comprising a combination of elements including, *inter alia*, "a cylindrical substrate having wirings formed thereon; and at least one semiconductor chip mounted on a circumferential surface of said substrate ... having bumps in contact with the wirings." Claim 13 is directed to a semiconductor device including, *inter alia*, similar recitations.

Sharp is directed to a semiconductor device formed on a flexible film-like insulating substrate. Sharp illustrates a semiconductor role chip 1, in which a thermoelectric semiconductor 3 is formed on a film-like insulating substrate 2. Sharp, Fig. 2. Thermoelectric semiconductor 3 comprises a P-type heat conversion semiconductor and a N-type heat conversion semiconductor. Sharp, Abstract.

The Examiner alleges that thermoelectric semiconductor 3 corresponds to a plurality of stacked semiconductor chips "mounted on the circumferential surface of [a cylindrical] substrate," (Office Action, p. 2). However, thermoelectric semiconductor 3 is formed directly on insulating substrate 2. *See* Sharp, Fig. 2. Since thermoelectric semiconductor 3 is directly formed on substrate 2, the semiconductor device disclosed by Sharp does not include wirings and bumps as recited in claims 1 and 13. Thus, Sharp fails to anticipate claims 1 and 13 because Sharp fails to teach all the claim elements. For at least this reason, claims 1 and 13 are allowable.

Claims 2-11 are allowable at least due to their dependence from allowable claim 1. Claims 16, 17, and 20 are allowable at least due to their dependence from allowable claim 13.

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Furthermore, claim 26 is directed to method of manufacturing a semiconductor device comprising a combination of elements including, *inter alia*, "mounting at least one semiconductor chip having bumps on at least a region" (emphasis added). As advanced above, Sharp fails to disclose at least a semiconductor chip having bumps. Thus, Sharp also fails to teach at least "mounting at least one semiconductor chip having bumps." Therefore, Sharp fails to anticipate claim 26 because Sharp fails to teach all the claim elements. For at least this reason, claim 1 is allowable.

II. Buck

Buck is directed to a side tap assembly of a coaxial electric signal cable. Buck illustrates that pins 16 and 17 are arranged on the side surface of the coaxial electric signal cable and that an integrated circuit chip 19 is connected to pins 16 and 17. Buck, Fig. 3. The Examiner alleges that integrated circuit chip 19 corresponds to a semiconductor chip mounted on a cylindrical substrate 5 (Office Action, p. 3). Contrary to the Examiner's allegations, Buck differs from the invention recited in claims 1 and 13.

Buck relates to a coaxial electric signal cable, but does not disclose a combination of a cylindrical substrate having wirings and a semiconductor chip, or multilayered semiconductor chips, having bumps. The device illustrated in Fig. 3 of Buck comprises a conductive braid shielding 3 and conductive area 18, both of which are electrically connected to pins 17, not bumps. Moreover, conductive braid shielding 3 and conductive area 18 do not correspond to wirings and bumps as recited in claims 1 and 13. Thus, Buck fails to anticipate claims 1 and 13 because Buck fails to teach all the claim elements. For at least this reason, claims 1 and 13 are allowable.

Furthermore, the Examiner admits that "Buck does not appear to disclose a plurality of chips stacked one upon the other to form a stacked body on a surface of said

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substrate, or a plurality of stacked bodies arranged at predetermined distance apart in the outer circumferential direction of said substrate," and that "Buck does not appear to show a chip sealed with a resin" (Office Action, p.3, ¶ 10-12). The Examiner takes "Office Notice" that these features are "obvious to one of ordinary skill in the art," (Office Action, p.3, ¶ 10-12).

Applicant asserts that such allegations are improper in a rejection under 35 U.S.C. § 102. For anticipation under 35 U.S.C. § 102(b), each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. *See* M.P.E.P. § 2131, pp. 2100-68 to 69. Furthermore, rationale based on common knowledge in the art or "well-known" prior art (i.e. "Office Notice"), while applicable to a obviousness rejection (in certain cases), is not applicable to an anticipation rejection. M.P.E.P. § 2144.03, pp. 2100-129 to130. Since the Examiner admits certain elements are not disclosed by Buck, the rejection of claims 1, 12, 13, 14, 18, 19, 21-23 under 35 U.S.C. § 102(b) is improper. Thus, Applicant requests that the Examiner withdraw this rejection and allow the pending claims.

Allowable Subject Matter

The Examiner objected to claim 25 as being dependent upon a rejected base claim, but indicated that it would be allowable if rewritten in independent form including all the recitations of the base claim and any intervening claims. Applicant thanks the Examiner for indicating allowable subject matter. By this Amendment, Applicant rewrites claim 25 in independent form including all the elements of claim 24 from which it depended. In view of this, Applicant requests that the Examiner withdraw the objection to claim 25.

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In view of the foregoing, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Attached hereto is a marked-up version of the changes made to the claims by this Amendment. The attachment is captioned "**Appendix to Amendment of September 19, 2002**".

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: September 19, 2002

By: _____
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Appendix to Amendment of September 19, 2002

1. (Amended) A semiconductor device, comprising:

a cylindrical substrate having wirings formed thereon; and

at least one semiconductor chip [formed] mounted on [the] a circumferential surface of said substrate, said semiconductor chip being bent along the surface of said substrate and having bumps in contact with the wirings.

2. (Amended) The semiconductor device according to claim 1, wherein a plurality of semiconductor chips are mounted to [the] an outer circumferential surface of said substrate a predetermined distance apart from each other in [the] an outer circumferential direction of said substrate.

3. (Amended) The semiconductor device according to claim 1, wherein a plurality of semiconductor chips are mounted to [the] an outer circumferential surface of said substrate a predetermined distance apart from each other in [the] a longitudinal direction of said substrate.

4. (Amended) The semiconductor device according to claim 1, wherein said semiconductor chip is arranged to cover [the] an entire outer circumferential surface of said substrate.

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5. (Amended) The semiconductor device according to claim 1, wherein said semiconductor chip is arranged on [the] an inner circumferential surface of said substrate.

6. (Amended) The semiconductor device according to claim 1, wherein a plurality of semiconductor chips are arranged on [the] an inner circumferential surface of said substrate a predetermined distance apart from each other in [the] an inner circumferential direction of the substrate.

7. (Amended) The semiconductor device according to claim 1, wherein a plurality of semiconductor chips are arranged on [the] an inner circumferential surface of said substrate a predetermined distance apart from each other in [the] a longitudinal direction of the substrate.

8. (Amended) The semiconductor device according to claim 1, wherein said semiconductor chip is arranged over [the] an entire inner circumferential surface of said substrate.

9. (Amended) The semiconductor device according to claim 1, wherein said semiconductor chips are arranged on both [the] an outer circumferential surface and [the] an inner circumferential surface of said substrate.

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10. (Amended) The semiconductor device according to claim 1, wherein [the] an outer circumferential surface of said substrate is sealed with a resin layer.

12. (Amended) The semiconductor device according to claim 1, wherein a plurality of terminals for connection are arranged in one edge portion in [the] a longitudinal direction of said cylindrical substrate, and said terminals are electrically connected to said semiconductor chip.

13. (Amended) A semiconductor device, comprising:

a cylindrical substrate having wirings formed thereon; and

at least one stacked body [formed] mounted on [the] a circumferential surface of said substrate, said stacked body including a plurality of semiconductor chips stacked one upon the other and being bent along the surface of said substrate, wherein each of said semiconductor chips has bumps, and the bumps formed on one of said semiconductor chips are connected to said wirings.

14. (Amended) The semiconductor device according to claim 13, wherein a plurality of said stacked bodies are [arranged] mounted to an outer circumferential surface of said substrate a predetermined distance apart from each other in [the] an outer circumferential direction of said substrate.

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15. (Amended) The semiconductor device according to claim 13, wherein a plurality of said stacked bodies are arranged a predetermined distance apart from each other in [the] a longitudinal direction of said substrate.

16. (Amended) The semiconductor device according to claim 13, wherein said stacked body is arranged to cover [the] an entire outer circumferential surface of said substrate.

17. (Amended) The semiconductor device according to claim 13, wherein said stacked body is arranged on [the] an inner circumferential surface of said substrate.

18. (Amended) The semiconductor device according to claim 13, wherein a plurality of stacked bodies are arranged on [the] an inner circumferential surface of said substrate a predetermined distance apart from each other in [the] an inner circumferential direction of the substrate.

19. (Amended) The semiconductor device according to claim 13, wherein a plurality of stacked bodies are arranged on [the] an inner circumferential surface of said substrate a predetermined distance apart from each other in [the] a longitudinal direction of the substrate.

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20. (Amended) The semiconductor device according to claim 13, wherein said stacked body is arranged over [the] an entire inner circumferential surface of said substrate.

21. (Amended) The semiconductor device according to claim 13, wherein said stacked bodies are arranged on both [the] an outer circumferential surface and [the] an inner circumferential surface of said substrate.

22. (Amended) The semiconductor device according to claim 13, wherein [the] an outer circumferential surface of said substrate is sealed with a resin layer.

23. (Amended) The semiconductor device according to claim 13, wherein a plurality of terminals for connection are arranged in one edge portion in [the] a longitudinal direction of said cylindrical substrate, and said terminals are electrically connected to said semiconductor chip.

25. (Amended) [The method of manufacturing a semiconductor device according to claim 24,] A method of manufacturing a semiconductor device, comprising:

bending at least one semiconductor chip; and

mounting the bent semiconductor chip on at least one region of the surface of a cylindrical substrate,

wherein said semiconductor chip is held by a holder having a curved surface in said bending step.

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26. (Amended) A method of manufacturing a semiconductor device, comprising [the steps of]:

mounting at least one semiconductor chip having bumps on at least a region of [the] a surface of a flexible substrate; and

bending said substrate into a cylindrical form.

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